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In the Claims:

Please amend claims 1-3, and add new claim 12 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A thin film Silicon on Insulator (SOI) device comprising:

a source₁[[,]]

a gate₁[[,]]

a drain₁[[,]]

an SOI layer₁, and

a substrate layer₁

an insulator layer between the SOI layer and the substrate layer, wherein when the substrate layer being is maintained at a potential enough sufficiently lower than a potential of the source so that a parasitic MOS channel is formed between the source and drain; and

a Deep N implant layer formed between either the source or drain and the insulator layer parasitic MOS channel to prevent the flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

2. (Currently Amended) The device of claim 1 wherein the Deep N implant layer is formed between the source and the insulator layer parasitic MOS channel.

3. (Currently Amended) The device of claim 1 wherein the Deep N implant layer is formed between the drain and the insulator layer parasitic MOS channel.

4-11 (Cancelled)

12. (New) The device of claim 1, wherein the substrate layer is maintained at a potential that is about 200 volts lower than the potential of the source.